CONCLUSION & FUTURE SCOPE

The chapter concludes the research work with conclusion and small discussion is also done on future work and ended with the references used to support the research work in nice manner.

7.1 Conclusions

NoC is the network version of any communication chip and new approach to provide signaling and environment to utilize the efficient interconnections and link with the verification of current system on chips. NoC based design are helpful in reduction of the extra hardware used in the design and complex chips interconnections. The low and slow band signals are grouped and multiplexed over a single line and larger bandwidth signals can communication directly using high speed in 2D and 3D topology with parallel paths or ports. The NoC communication of the network is done in 2D mesh, 2D torus, 2D ring and 2D fat tree topology using 2D router. The 2D router has 5 parallel ports to communicate. The NoC communication of the network is done also for 3D mesh, 3D torus, 3D ring and 3D fat tree topology using 3D router. The 3D router has 7 parallel ports to communicate. The chip design, simulation and synthesis of the 2D mesh, 2D torus, 2D ring and 2D fat tree NoC is done for cluster size (N= 2, 4, 8, 16, 32, 64, 128, 256). In the same way the chip design, simulation and synthesis of the 3D mesh, 3D torus. 3D ring and 3D fat tree NoC is done for cluster size (N= 2, 4, 8, 16, 32, 64, 128, 256). The data transfer for the 2D NoC and 3D NoC is verified with the destination node and intercommunicating network. The results are verified for different test cases under data transfer scheme.

- In comparison to the 2D and 3D topological structure, 3D NoC is more efficient and reliable because the data

can be received by 3D router using 7 parallel ports and scheduling is possible

- The hardware utilization and related parameters such as slices, flip-flops, LUTs and Input and output blocks IOBs of 2D mesh, 2D torus, 2D ring and 2D fat tree topology is increasing with the increase in network configuration or the cluster size of the network (N= 2, 4, 8, 16, 32, 64, 128, 256).
- The hardware utilization and time related parameters such as slices, flip-flops, LUTs and Input and output blocks IOBs of 3D mesh, 3D torus, 3D ring and 3D fat tree topology is increasing with the increase in network configuration or the cluster size of the network (N = 2, 4, 8, 16, 32, 64, 128, 256).
- The hardware utilization, memory and timing values/ delay are obvious because network configuration or size is increasing.
- The frequency support and memory usage is also increasing with network cluster (N= 2, 4, 8, 16, 32, 64, 128, 256).
- 3D mesh topology has less hardware, memory utilization, flip flops, slices, LUTs in comparison to other topology such as 3D torus, 3D ring and 3D fat tree topology.
- The frequency support in FPGA hardware for 3D mesh topology is larger in comparison to 3D torus, 3D ring and 3D fat tree topology. It guarantees the designed chip will be more faster in comparison to 3D torus, 3D ring and 3D fat tree topology.
- The router design, FPGA implementation of 2D and 3D mesh is scalable in comparison to other topology. The regular design and structure feature of the mesh NoC is the greatest attraction of all designer because there may be another possible link in case of the failure of the specific link for internode communication. Nodes are placed on the equal distance and address by XYZ routing.

The hardware implementation is a great revolution in the chip technology to optimize the hardware and to configure the programmable interconnects. The main advantage of the programmable structure is that we can identify the faulty node and replace the node easily with configurable structure. From the device utilization parameters and timing parameters it is concluded that 3D mesh has the optimal design, switching capability and higher response comparison to ring NoC. It signifies that torus, ring and fat tree NoC consumes more memory and hardware in comparison to mesh 3DNoC. The frequency support of 3D mesh NoC is larger in comparison to NoC. Hence mesh NoC has faster response in comparison to ring NoC. The geographical area covered by the ring NoC is larger than mesh NoC. Hence it supports the wide band width and coverage. Mesh NoC crossbar structure and has addressing based on row and column address. The geographical area covered by mesh NoC is less than ring NoC. Overall the performance, speed, hardware utilization of developed 3D mesh NoC is the best solution for the development of large scale and programmable switching networksand the industries will be benefited by the research working in the field of computer networks and programmable architectures for the implementation of specific network

7.2 Future Work

In future, we can configure the more number of nodes in 2D and 3D network structures. The number of networks for intercommunication in 2D and 3D NoC can also be increased based on network selection logic. We can implement the same concept for specific wireless sensor network. We can also add the features of security by encryption and decryption of data transfer among nodes. The chip design and development of programmable NoC is a great revolution for implementing programmable switches, reconfigurable NoC and multimedia networks. It is also possible to develop the NoC for wireless communication. The proposed architecture is applicable for inter and intra communication among networks.