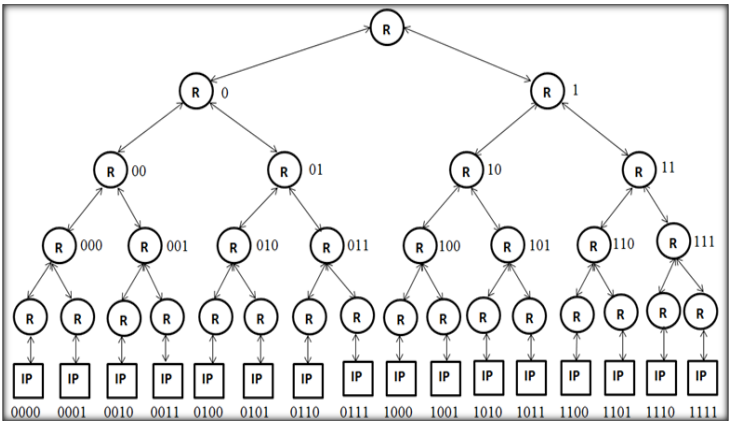

Figure 4.12 Structured fat tree NoC for 16 nodes

In the same way each router associated with third stage routers which are "000", "001", "010", "011", "100", "101", "110" and "111". In the last stage the sub routers are associated with their IPs. The communication for the 16 nodes form parent to child nodes or routers is possible in indirect way in the same tree the nodes are identified as "0000" node0, "0001" node1, "0010" node2 and so on.

Methodology and Implementation

The chapter explains the research methodology and software tools description from simulation as well as synthesis. It also details the complete environment of functional simulation and logic verification

5.1 Software Tools

The software used in the design of NoC and the chip implementation used is Project Navigator Xilinx ISE 14.2 and Modelsim 10.0 software

5.1.1 Xilinx ISE Project Navigator 14.2

Xilinx is one of the leading companies in the field of SCI and FPGA design. It is the biggest semiconductor company to cover the front end solutions in the chip design, verification and synthesis. In the Xilinx software the programmers are developing the chip using latest HDL languages such as Verilog HDL, VHDL, and ABEL etc. After the design there are the options to see the RTL, inter schematic view and view synthesis report. The developed chip is configured using input pins, output pins and input/output pins. Xilinx has the ISIM simulator to see the waveform using inbuilt waveform simulator which provides the functional check of the developed chip. It also has the Chip scope for FPGA signal analysis, Static timing analysis feature, verification and logical synthesis environment. Different test benches and test cases are simulated in the software environment and FPGA guarantees the chip for mask production in the market. The tool provides the full information of logic design, synthesis, simulation, and verificationand timing analysis. The hardware and pre-synthesis parameters obtained directly from the tool which details the hardware parameters usage, memory requirements and timing values required in the design of chip.

5.1.2 ModelsimSoftware 10.1 Version

Modelsim Software is the software given by the Mentor Graphics Company. It is a multi-language HDL simulation software works on Verilog HDL, VHDL and System 'C'. It has the inbuilt 'C' debugger. It is preferred one of the best tool for GUI and Xilinx software interface. The chip design, functional simulation and timing analysis are done using the software. It also can be integrated with MATLAB or Simulink environment. The software gives the following advantages

Benefits of Modelsim EE

- Modelsim software gives low cost chip design solution using HDL
- Providing interactive debug using Intuitive GUI in effective time
- It simplifies the research data and manages the project management integrated in software and hardware
- It has outstanding technical support to give the solutions in HDL and easy to use
- Easy to use with outstanding technical support
- Popular ASIC libraries are available and sign-off support for all defined libraries
- The complete platform for hardware and software debugging
- Simplifies the functional simulation and gives testing environment for all the possible test cases, can be used to check the functionality of the designed chip.

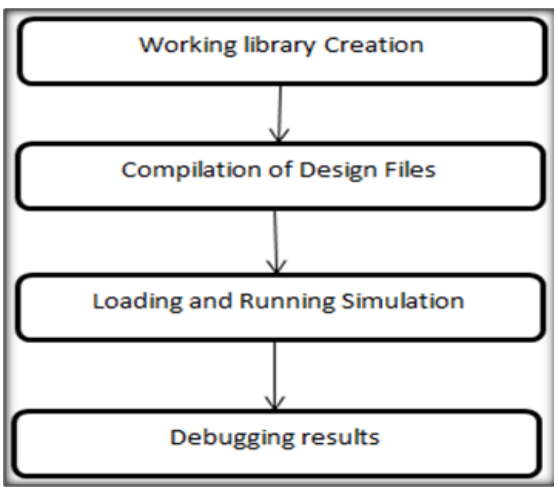

Figure 5.1 Modelsim design process

The chip design flow and simulation block diagram using Modelsim software is shown in fig. **5.1**

- Creation of working library:All the chip design based solutions in Modelsim software require the creation of the library. There is the default library in the Modelsim by the name 'work' which includes all the logical values and possible library functions required to do simulation by the compiler in the working library. The default destination of all the chip design is the library in Modelsim software.

- Designed file compilation:The designed which is developed using any HDL, and stored in the working library is complied. The binary created by the user is suited to work on all the platforms. The designed file may be one file or grouped as the top design having sub modules or structured in bottom to top level.

- Running and loading Simulation: The designer is loading the top module of the developed chip into the simulator after completing the compilation of the design. The loading involves the entity of chip and architecture. The design can be done in dataflow, behavior and structural modeling. The modeling of the design is choosen by the designer. Some design structured using structure style of modeling, gives better results. The design is developed in different modeling can give different timing and performance results. In the running process, it is considered that the simulation period is zero and run operations are entered by the designer to perform the functional simulation

- Results debugging:The developed chip may contain some errors. So, debugging environment is required to track the errors in program window. The errors are listed by the modelsim with respect to line and code debugging environment help the program to check the code and take correct action in design. There are redefined scripts can be used in the software to follow the short methods.

The verified results are seen in the form of waveform and timing diagrams.

5.2 Methodology

Multiple steps are required in the NoC design.The methodology has the several steps used to design the chips for topological architectures.

- Design Specification: There are two approaches in the NoC design one is bottom up design another is top-down approach. In the bottom up technique the design is developed for small modules and structured in a top design using structural style of modeling. In top –bottom up approach the full system is considered and designed in a way that it will meet the behavior of the system.

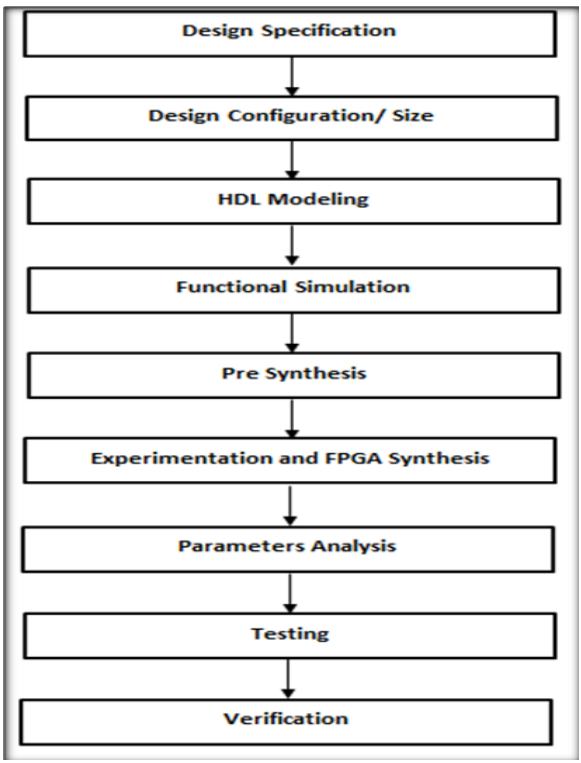

Figure 5.2 NoC design methodology

- Design Configuration:In the NoC design of ring, torus, mesh and fat tree topology is of the cluster size. The topology design can vary with the cluster size and topology behavior in 2D and 3D. The design specifications are decided by the designer based on company/ project requirement.

- HDL Modelling:The chip design is done using any of the HDL language. The industry favorite languages are Verilog HDL and VHDL. In our design of 2D and 3D topological NoC, VHDL based design is used for the problem statement of our research because the NoC design can be modeled in dataflow modeling, behaviour modeling or structured modeling using this language.

- Functional Simulation: The functional simulation depends on reset circuitry, clock input and test cases. The designed chips and modules are checked by RTL view, internal schematic diagram and test cases. Test cases are decided by the designer based on the functionality of the designed chip.

- Pre Synthesis:In the parenthesis the NoC performance is analyzed based on the hardware and timing parameters. The hardware parameters are slices, flip-flops, LUTs and memory requirements in the chip. The timing parameters are relating to combination delay, minimum time and maximum time of clock etc. The timing parameters are relating to combination delay, minimum time and maximum time of clock etc. If any chip design is consuming the memory more than 100% utilization, then chip redesigning is required.

- FPGA Synthesis and Experimentation:Based on the view synthesis report as the hardware and device utilization summary the designed modules are synthesized on FPGA. The FPGA is interfaced with the computer in which the code was developed for specific NoC. The test inputs are given using switches of the board and verified

using LED, LCD or monitor using VGA. FPGA has the feature of inbuilt ADC and DAC conversion. So, FPGA synthesis and experimentation is required to test the designed chip in real time application. In the NoC design experimentation is done on Vertex 5, high speed FPGA.

- Parameters Analysis:The NoC design parameters analysis is must and required to check step by step weather the hardware and other related parameters are consuming unbalanced number of resources. In NoC design the parameters analysis is done based on the cluster size and configuration.

- Testing:FPGA accepts the inputs in the form of LUTs. The synthesized results are checked and tested successfully on FPGA. In the NoC design, main testing is done for the input signal processed by the FPGA or not. FPGA input and output signal can be checked with the help of Chip scope inbuilt in the Xilinx ISE Software.The signals can be checked on CRO or DSO because the FPGA can be interfaced with DSO because it has inbuilt ADC and DAC that provides this feasible solution. The testing is also done in software and data is checked in the input signals and processed properly. The assignment of the source router address, destination router addresses and data size are the essential part in each NoC.

- Verification: Standard VHDL Programming has all the features required to check and verify the stimuli, randomization and functional coverage. It is essential in NoC because it directly relating to clear cluster size of the network. The nodes can discontinue their link, routing. There should be alternate route, path, and links for full available NoC communication. The data communication the destination nodes is checked by 2D and 3D mesh, ring, torus and fat tree topology. The verification of NoC is done using timing parameters and different possible test cases of the developed chip called design under test (DUT).