TOPOLOGY DESIGN AND INTERCOMMUNICATION

The chapter focuses on the designing of 2D and 3D topological configuration with different cluster size. The chapter also discusses the designing of 2D and 3D mesh, torus and ring topological structure and their behavior in intercommunication.

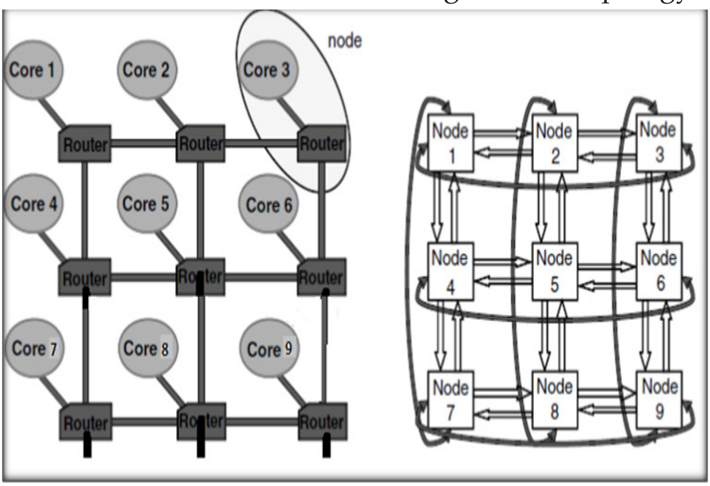
4.1 Introduction to Network Topology

Many applications need the architectures which are based on bus topological structures and bus based architectures may be used to prevent the performance of these systems, as there is the increment in Systems-on-Chips (SoCs) based IP modules. The systems which are generally use bus based communication, are not able to meet the requirement of bandwidth, power consumption and latency. Network on Chip (NoC) is the solution for such communication based system, which is a bottleneck for an embedded switching network to interconnect the different IP modules in SoCs. In comparison to the bus based communication system, the bandwidth and design space is larger to maintain the arbitration mechanism and routing algorithms and their implementation strategies with different communication infrastructure. Moreover, NoC are very much helpful for fault tolerance and enable to SoC design engineers to search the suitable solutions for several system constraints and characteristics. The NoC is characterized by different structure and routers connection. The way of connected the different routers and their organization is called the topology and can be represented on the graphical forms. Topology graph G (N, C) in which

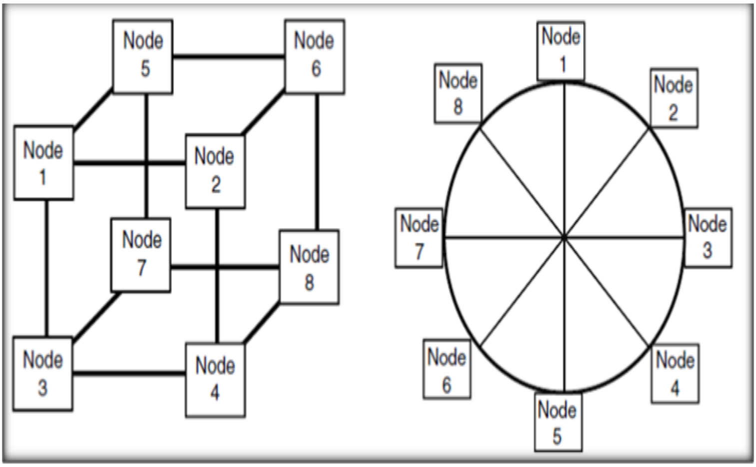
N -> set of the routers

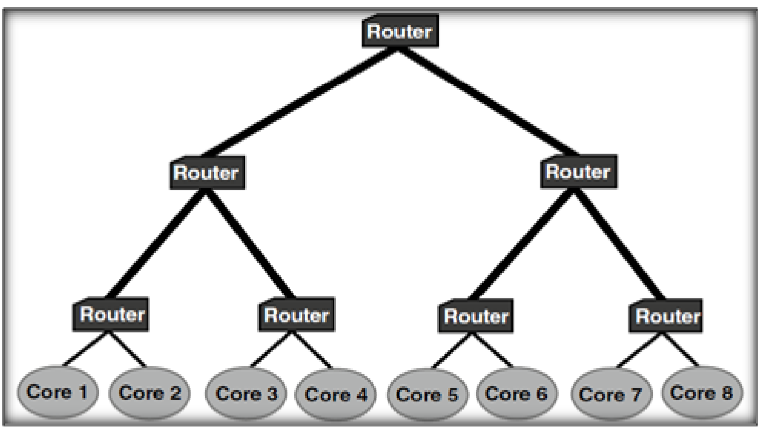
C -> set of the communication channels

The routers can be connected in the direct topology and indirect topology. In the direct topology all the routers are associated with the processor and their combination can be used as a single processing element in the system referred as the nodes in the communication network. In the direct topology the nodes are directly connected to the neighboring nodes with fixed length and messages transferred among the nodes directly with the help of one or more immediate nodes. The communication is taking place according to the different routing algorithms among the routers and routers are directly involved in the communication throughout the topology.



(a) 2D mesh (b) 2D torus





(e) Fat tree

Figure 4.1 Topological Structures

Most of the structured are based on the orthogonal arrangement with in the routers and nodes are scattered in N- Dimension and data packets moves in a dimension at a particular time. Such types of arrangement are trade-off between performance and cost and give the scalable and programmable architecture. Most of the popular topologies are N- Dimension mesh, torus and hypercube. The 2D mesh topology is configured in XY structured where x represents the row and y represents the column. It is assumes that all the link have the same length to imposes the regular structure used in physical design for simplification. It is also easy to predict that the space or area required for the designing of mesh topology. One more reason is also that the topology grows almost in the linear nature with the increment in the number of the nodes in XY direction. The advantage of the mesh topology over the other is due to its structure linearity and physical design. It has also some disadvantage as router used in the mesh topology can lead the consisted region in the NoC. Due to this problem design has to take lot of care that the design and application should be mapped to avoid the traffic and concession especially in the center region of the mesh.

Fig. 4.1(a) to (e) shows the direct and indirect topology. The fat tree is the indirect topology as depicted in fig 4.1(e). In indirect topology all the routers are not connected in direct manner as in mesh, torus or ring. The source and target nodes are connected in indirect way such as in multistage networks, crossbar switch and tree structures. The tree topology follows the parent- child relation to connect the source to target node.

4.2 Mesh Topology

In computer network, a crosspoint switchis also referred as crossbar switch, or a switching matrix that provides multiple inputs to multiple outputs in the form of matrix. 2D NoC router follows the cross point switch. The mesh NoC is the structured form if m x n size routers. The data is processed by the nodes. Each node is consist of its own processing element. One node can communicate to another with the help of router. The m x n size of the NoC presents that the nodes can are identified by X direction and Y direction with the size of m x n. For an example, let us consider 4 x 4 mesh architecture as shown in fig. 4.2. To address 16 routers ($2^n = 16$, $n = 4$ bit) addressing is required in which 2 bit address in taken care on X axis and 2 bit address on Y axis. The selection of the routers is done based on the cross point addressing as listed in table 4.1. It is called the XY routing of the 2D mesh network in which X axis presents the row address and Y axis presents the column address. To understand the detailed behavior of the 2D mesh NoC, another example of 64 nodes ($2^n = 64$, then $n = 6$ bit) is also depicted in fig. 4.3 which is identified by 3 bit address in X axis direction as row address and 3 bit address in Y axis direction in column address. The node addressing for nodes is listed in table 4.3. In the mesh NoC it is considered that all the nodes are placed on equal distance and configured or arranged in regular structure.

Table 4.1 2D Mesh routing using XY

Source_address		**Destination**
X	Y	Router Selection
00	00	Acknowledgment to Router R0
00	01	Acknowledgment to Router R1
00	10	Acknowledgment to Router R2
00	11	Acknowledgment to Router R3
01	00	Acknowledgment to Router R4
01	01	Acknowledgment to Router R5
01	10	Acknowledgment to Router R6
01	11	Acknowledgment to Router R7
10	00	Acknowledgment to Router R8
10	01	Acknowledgment to Router R9
10	10	Acknowledgment to Router R10
10	11	Acknowledgment to Router R11
11	00	Acknowledgment to Router R12
11	01	Acknowledgment to Router R13
11	10	Acknowledgment to Router R14
11	11	Acknowledgment to Router R15

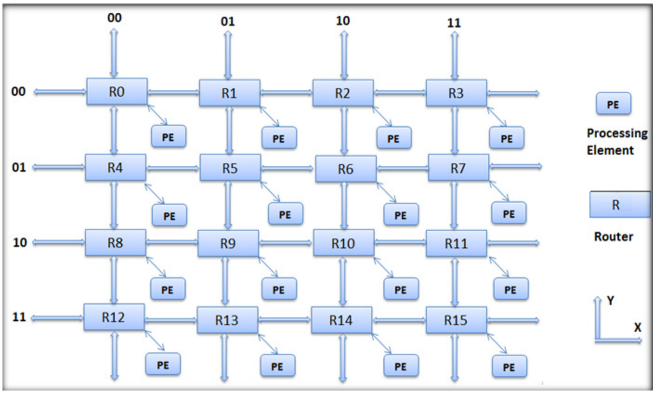


Figure 4.2 Mesh Configuration (4 x 4)

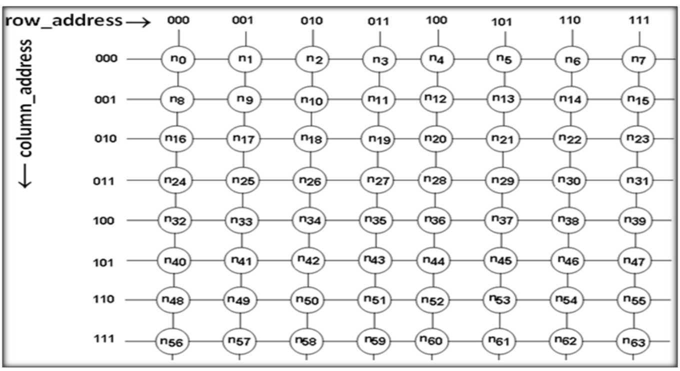


Figure 4.3 Mesh Configuration (8 x 8)

Table 4.2 Router identification in 2D_mesh network

X_ Address	Y_ address	Destination Router
000	000	Router 0
000	001	Router 1
000	010	Router 2
000	011	Router 3
000	100	Router 4
000	101	Router 5
000	110	Router 6
000	111	Router 7
001	000	Router 8
001	001	Router 9
001	010	Router 10
001	011	Router 11
001	100	Router 12
001	101	Router 13
001	110	Router 14
001	111	Router 15
010	000	Router 16
010	001	Router 17
010	010	Router 18
010	011	Router 19
010	100	Router 20
010	101	Router 21
010	110	Router 22
010	111	Router 23
011	000	Router 24
011	001	Router 25
011	010	Router 26
011	011	Router 27
011	100	Router 28
011	101	Router 29
011	110	Router 30
011	111	Router 31
100	000	Router 32
100	001	Router 33
100	010	Router 34
100	011	Router 35
100	100	Router 36
100	101	Router 37
100	110	Router 38
100	111	Router 39
101	000	Router 40

101	001	Router 41
101	010	Router 42
101	011	Router 43
101	100	Router 44
101	101	Router 45
101	110	Router 46
101	111	Router 47
110	000	Router 48
110	001	Router 49
110	010	Router 50
110	011	Router 51
110	100	Router 52
110	101	Router 53
110	110	Router 54
110	111	Router 55
111	000	Router 56
111	001	Router 57
111	010	Router 58
111	011	Router 59
111	100	Router 60
111	101	Router 61
111	110	Router 62
111	111	Router 63

In the general way, a matrix switch configured structure is formed with the help of a grid of crossing metal bars, and can be broadened in matrix form as crossbar switch. It is one of the original switching architectures, memory switch together with a rotating switchand a crossover switch Using crossbar switches up to 'N' CPU's can be connected. In case of same topological from, more CPU's can be connected and the network becomes too complicated and very expensive. Although the cluster size of n*k switches is needed for the crossbar switches connects 'n' no. of CPU's to 'k' memories of CPU's. We can understand the addressing and node selection scheme with the help of the functional table listed below. The selection of the source and destination subscriber depends on the X axis address and Y axis address. The value of XY is not fixed it is variable depending on the number of input and output nodes. For the considered case, it has been taken 3 bitas row wise address and 3 bit columns wise to recognizes the node in 2D configuration.

The 3D mesh topology is also configured in the same manner as 2D mesh topology. In 2D mesh the routing is done based on XYZ. The diagram for Mesh (3 x 3 x 3) NoC in 3D is shown in [Figure 4.4]. In the design 27 routers can communicate. The packet information is depicted in [Figure 4.5]

End bit (1 bit): The status of the end bit is depicted about the ending of the transmission and it indicates that the data is received at the receiving end.

Layer Identification (3 bit): Multilayer environment is also supported by the 2D and 3D NoC. In layer identification, the addresses of the layers are identified. In our case it is assumed 3 bit, it means it can support 8 layers environment.

Sxyz (3, 3, 3) Source Router (9 bit): It denotes the address of source routers need to communicate based on XYZ routing. It is address as X (3 bit), Y (3 bit) and Z (3 bit) direction.

Dxyz (3, 3, 3) Destination Router (9 bit): It denotes the address of target routers to end the commutation as destination routers based on XYZ routing. It is addressed as X (3 bit), Y (3 bit) and Z (3 bit) direction.

Data (n bit): It indicates the size of the data. It may be of 'n' bit in our case it assumed of 0 to 255 or 256 bit data.

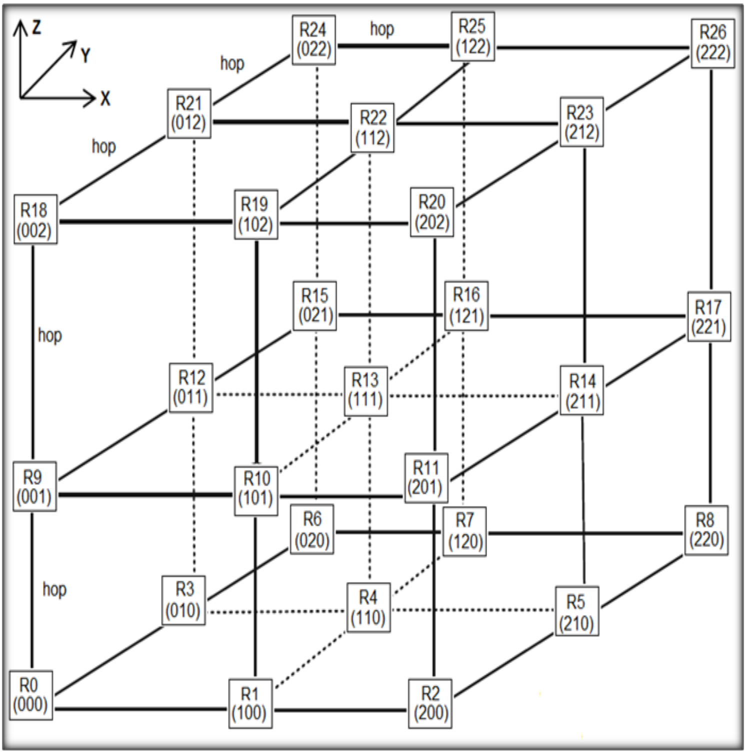


Figure 4.4 Mesh (3 x 3 x 3) NoC in 3D

End bit	Identification _ Layer	Router Source Sxyz (3, 3, 3)	Router_ Destination Dxyz (3, 3, 3)	Data (n bit)
(1 bit)	(2 bit)	(9 bit)	(9 bit)	(256 bit)

Figure 4.5 Data packet format

Table 4.3 Mesh 3D (3 x 3 x 3) NoC under XYZ routing

X_address	Y_address	Z_address	Router Selection	XYZ Routing
000	000	000	Acknowledgment to Router R0	(000)
001	000	000	Acknowledgment to Router R1	(100)
010	000	000	Acknowledgment to Router R2	(200)
000	001	000	Acknowledgment to Router R3	(010)
001	001	000	Acknowledgment to Router R4	(110)
010	001	000	Acknowledgment to Router R5	(210)
000	010	000	Acknowledgment to Router R6	(020)
001	010	000	Acknowledgment to Router R7	(120)
010	010	000	Acknowledgment to Router R8	(220)
000	000	001	Acknowledgment to Router R9	(001)
001	000	001	Acknowledgment to Router R10	(101)
010	000	001	Acknowledgment to Router R11	(201)
000	001	001	Acknowledgment to Router R12	(011)
001	001	001	Acknowledgment to Router R13	(111)
010	001	001	Acknowledgment to Router R14	(211)
000	010	001	Acknowledgment to Router R15	(021)
001	010	001	Acknowledgment to Router R16	(121)
010	010	001	Acknowledgment to Router R17	(221)
000	000	010	Acknowledgment to Router R18	(002)
001	000	010	Acknowledgment to Router R18	(102)
010	000	010	Acknowledgment to Router R20	(202)
000	001	010	Acknowledgment to Router R21	(012)
001	001	010	Acknowledgment to Router R22	(112)
010	001	010	Acknowledgment to Router R23	(212)
000	010	010	Acknowledgment to Router R24	(022)
001	010	010	Acknowledgment to Router R25	(122)
010	010	010	Acknowledgment to Router R26	(222)

4.3 Torus Topology

The torus topology is formed by the revolution of a circle on axis to the circle as a coplanar. In 2D planner topology the degree of freedom is 4and the nodes can the configured in 2D rectangular lattice shape with m x n size means m is the number of rows and n is the number of columns with four neighbours as connecting nodes. The rectangular array can be rolled out and the opposite side nodes can be visualized by rolling the nodes array structure. The 2D torus (4 x 4) is shown in fig. 4.6. The nodes can communicate in +X, +Y, -X and –Y direction. In case of the 3D torus nodes the network is configured in a shape that can shape a rectangular prism with 6 degree of freedom or directions +X, +Y,+Z –X,-Y and –Z directions. The example of 3D torus is depicted in fig. 4.7. The addressing of 2D torus and 3D torus is based on XY and XYZ routing discussed in mesh topology.

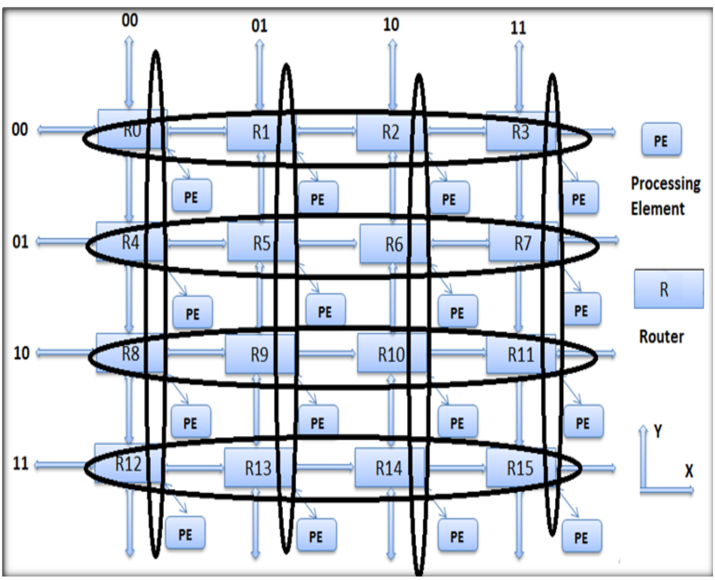


Figure 4.6 Torus (4 x 4) Topology in 2D shape

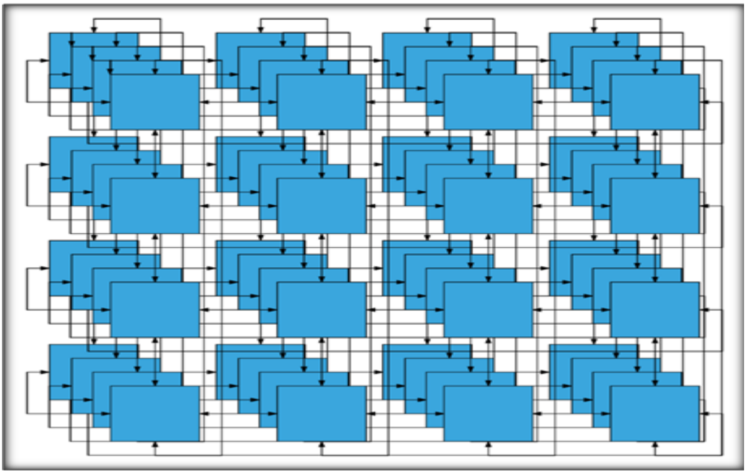


Figure 4.7 Torus (4 x 4 x 4) Topology in 3D shape

4.4 Ring Topology

Ring Topology is the well-known topology based on direct connections. The example of the ring NoC is Octagon which is the simple structure in which 8 nodes communicate to each other with the help of 12 interconnecting links. The Octagon is shown in fig. 4.8. The links are helping in the two ways communication of the structured NoC arranges in a ring shape. It is following the easy and simple algorithm to choose shortest path of routing. A switch is used to connect the nodes and establishes the communication in multidimensional shape. Fig. 4.9 shows the examples of 64 nodes are shaped in the ring form. To address 64 nodes in ring form the addressing of 6 bit is required. It is started from "000000" as M0 for node 0 and ended to "111111" M63 as node 63. Table 4.4 lists the addressing and behavior of router selection in the ring topological structure form node 0 to node 63 and corresponding routers as R0 to R63. All the nodes in the ring can communicate to each other. The node data packet has the data format in which source node and destination nodes address are kept of 6 bit each and 256 bit is the size of data.

The inter-process communication is done by the ring based NoC and corresponding architecture. Nodes are understood with the help of source address and destination address. For an example let node 1 want to communicate with node 15 then source address will be "000001" and destination node address will be "00001111". If a node wants to communicate with any one, it has the probability to communicate any of the target nodes as shown in fig. 4.10

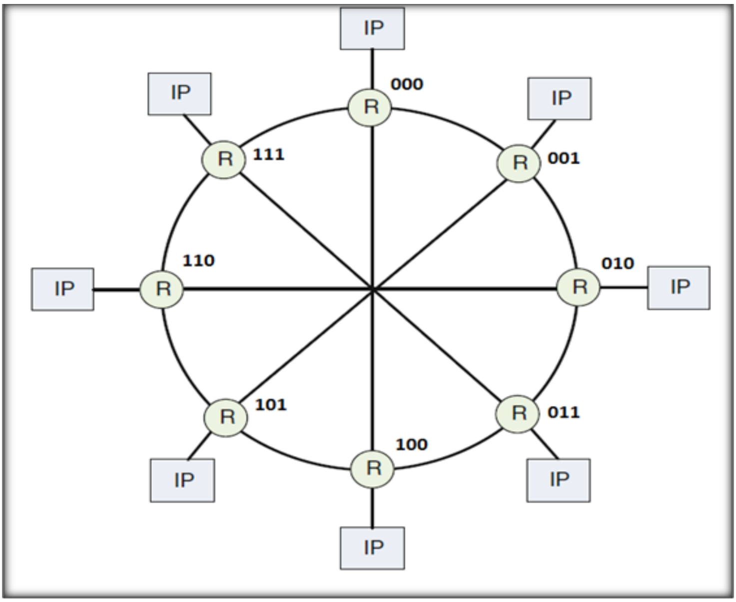


Figure 4.8 Ring NoC structured by 8 nodes

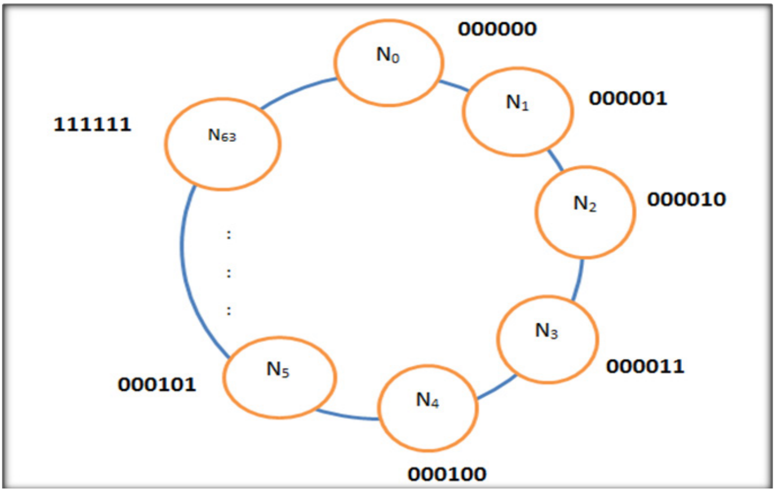


Figure 4.9 Ring NoC structured by 64 nodes

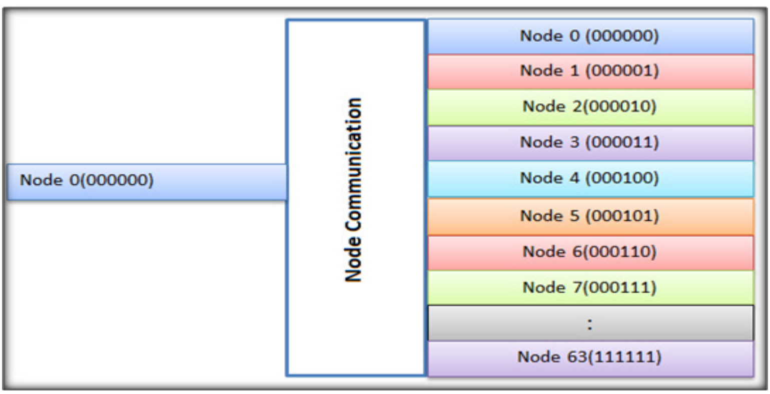


Figure 4.10 One node "0000" intercommunication to other nodes

Table 4.4 Node Identification scheme in ring NoC

Source_node(6 bit)	Destination_ node(6 bit)	Router Selection
000000 (Router 0)	000000:111111	Router 0 :Router 63
000001 (Router 1)	000000:111111	Router 0:Router 63
000010 (Router 2)	000000:111111	Router 0:Router 63
000011 (Router 3)	000000:111111	Router 0:Router 63
000100 (Router 4)	000000:111111	Router 0:Router 63
000101 (Router 5)	000000:111111	Router 0:Router 63
000110 (Router 6)	000000:111111	Router 0:Router 63
000111 (Router 7)	000000:111111	Router 0:Router 63
001000 (Router 8)	000000:111111	Router 0:Router 63
001001 (Router 9)	000000:111111	Router 0:Router 63
001010 (Router 10)	000000:111111	Router 0:Router 63
:	:	:
111111 (Router 63)	000000 :111111	Router 0:Router 63

The packet data is transmitted form the source router to target router. Fig. 4.11 shows the packet information having 6 bit defined for source router and 6 bit defined for target router. When the multiple requests are arriving to one of the destination, the priority based on FIFO logic is given to set the target nodes. The data of 'n' bit transfer is possible in ring NoC but in our case it is considered of 256 bit.

Source Router Address (6 bit)	Destination Router Address (6 bit)	Data value (n bit) (256 bit)

Figure 4.11Communication data format

4.5 Fat Tree Topology

Fat trees are the indirect topology network by Charles E. Lesierson suggested in 1985 in which the routers are connected in top to bottom in the form of tree. The tree structure has the advancement in its design that the links form the top to bottom and bottom to top are equal. The structure is based on the parent (root) and child, sub Childs relationship as siblings. It is the reason that the links are becoming "fatter" towards the top side of the tree. The switch in the root direction is having much number of links in comparison to the switch in the bottom side. The fat tree structure having 16 nodes in bottom is shown in fig 4.12.In the stage first, the router has two branches '1' and '0'. Two subunits (00, 01) are attached to the branch '0' and two sub units (10, 11)to branch '1'. In this four routers in stage two are addressed as"00", "01", "10" and "11".