REVIEW of LITERATURE

The chapter detailed the literature survey of the different researchers in the field of NoC, the findings of the survey and literature gaps are identified.

2.1 Literature Survey

The details of the some research papers are presented here.

Aurel A. Lazar in 1997 describe the comprehension on the exposed programmable networking model which is based on a fresh provision manner for the progressive telecommunication facilities that overcome on limitation over the current system of networks. This paper investigating the model will help us to clear the some major of the quarries antagonizing the telecommunication facilities industry. This paper focuses the program of switch implementation of the telecommunication networks. This paper focuses on the some important parameters like scalability, performance, Quality of Services, performance and applied matters. In this the paper exploits & tells us the benefits offered by Intellectual Properties and Asynchronous Transfer Machine technologies. It is a start of the era in programmable telecommunicating network and their reconfigurable structures.

Hiroaki Morino. et al. in 2002 describe about increasing the access use of the internet as well as the requirement of the speed up to tera byte of accessing the internet in the near future. Author shows a new paradigm of routing multilevel network for shortest path. The main advantage of this approach to make the simplicity of hardware and in this concept the switches has no buffer. A circuit of 8x8 nodes is proposed on file programmable gate array tool through which sixty-four by sixty-four circuit switch element is implemented in the one VLSI chips, and ten tera bits per second a switch

is realized by 2 phase interconnection additional the analysis work are often increased to implement a similar design on FPGA and validate the results when verify the segment communication. The comparison of the operative style and their performance parameters are often a boon for VLSI business. The performance parameters of the operative style embody minimum and most time, most output frequency, and hardware parameters admire resource utilization in terms of memory, logic gates, logic cells and no. of slices etc. in the last few years the speed of accessing the data is highly increased from kbps to mbps and now it has become mbps to tbps. Author has also discussed about the concept of single phase crossbar switch. My analysis work can target the implementation of the 3D mesh operative and different potential topological operative and compare the performance of all the operative and ring operative that underneath inter process communicating of VLSI chips. There is no buffer memory inside simple deflection routing crossbar switch as seen in multistage networks. Thus hardware simplicity is the most significant advantage of multistage network. Result of Xilinx simulation shows that this method can reduce hardware requirement in multistage networks when compare to conventional networks. Conventional close loop shuffle out switch by 10% resulting in rate of losing the packet is $5x10^{-7}$, sixty percent presented load in 64x64 switch. Switch elements of two types of circuit are floor planed on File Programmable Gate Array. Finally, the paper proposed the model for high capacity switches and the result of the simulator shows the reduction in the amount of hardware by the approximately ten percent.

Partha Pratim Pande et. al 2005 Authors suggested that the architectures based on the NoC topology are characterized by various trade-offs with regard to their specifications, performance, functionality and structure. They carried the work to compare and contrast the different architectures of the NoC to estimate the hardware parameters such as

latency, performance and power dissipation, and silicon area overhead. Some architecture are based on sustaining very high data rates at the cost of more energy dissipation and considerable overhead on silicon area, while others can suggests the lower data rate and lesser energy dissipation levels. Their main contribution lies in the illustration and establishment of a consistent and evaluation technique based on the set of quantifiable and readily parameters for NoCs.

Luciano Bononi et. al 2006 in this paper author analyse the several NoC topologies structure on modelling and simulation based. A uniform load is applied while the comparison is occurring among specially ring, mesh and spidergon topologies through the simulator. It has been observed that for the parallel processing the result is in the favour of the spidergon topology. Spidergon topology shoes the better performance and good scalability as compared to the others.

Muhammad Ali et. al 2006 as the growing complexity on the SoC a new paradigm NoC is introduced. Being introduced the new paradigm it is difficult to choose the appropriate simulator to check the efficiency of the NoC. Author used the NS2 for simulating the performance of the NoC. Authors describe the functionality of the NS2 tool.

Anderson Hansson. et. al in 2007 describe about the increasing the complexity on SOC (system on chip) with growing the intellectual properties integrated. A purely deadlock free concept is introduced that is UMARS known as 'unified mapping, routing and slot allocation'. An experiment has been applied on the MPEG decoder to judge the efficiency of the proposed algorithm, which result the reduction in NoC area by thirty-three percent and reducing in the power consumption by thirty-five percent. The author describe the introduction and related problem in section 2 and 3 respectively, and formalized in part number 4, section five consist the UMARS approach and finally section six consist the result which has been applied on the MPEG decoder. The main aim of this

paper to reduce two main things which are used to make the network totally deadlock free and completion of request constraints.

HyungGye et. al in 2007discussed the problem about the highly consistent on the system on chip due to increasing core. Author asked about the approached used traditionally that are bus system approach and point to point approach. However, the above approaches have low scalability, great complication, and rate and plan struggle. While the bus architecture can connect hundreds of core efficiently in terms of cost and complexity reduction. In this paper author perform a complete implementation on an application of multimedia that is MPEG-2 of P 2 P network, NoC and bus based topological network. The result shows that the consumption of the energy of NoC is less than the bus based and P to P.

TeijoLehtonen et. al. in 2007 emphasizes on the designing of the fault tolerance in NoC architecture. They developed several links that can tackle errors like transient, intermitted and permanent errors. Methods like hamming coding technique is used to realize the presence of transient error, interleaving method is used for error detection and Automatic Repeat Query method is used for recovery of the system. Sharing of information in the link is depend upon the signaling of two phase asynchronous while the lines of control have the responsibility to controlling Automatic Request repeat query. The functionality of the network is controlled by the control lines and the data is protected by using triple modular redundancy. Now, the developed design is judged against reference designs and co-operated. From the obtained result, it has been observed that efficiency of NoC decreases when compared to an ARQ design. But the reconfiguration structure is similar for divided communication strategy and extra cable strategy. The concept of Split communication has throughputtwenty-fivepercent, latencythirty-one percent and the latency of extra wire has fifteen percent while the throughput only ten percent.

Vasilis F. Pavlidis. et. al in 2007 describes the chip integration of 2D and 3D NoC topological designs. Several topological structures are introduced in 2-D and 3-D planes and the result has been compared on the several parameters like as the transaction speed and the power consumption. A processing element can be executed on a single physical plane. Thus, every 3D NoC has at least one PE on every physical plane and the total number of processing element on the system can be calculated as p1*p2*p3, and p1, p2, p3 represents the processing elements in the X, Y and Z plane respectively. The adjustment of nodes on 2D and 3D plane is described in this paper. A 3D NoC topology is proposed, which contains one PE. Each and every PE can be integrated in multiple planes. Thus it becomes possible to construct a 3D hybrid NoC. In such a system, both 2D and 3D NoC can stay together on one physical plane of the system. The paper tells us about the NoC topologies with the consideration of zero load model. The different parameters are compared in both the plane either 2-D or 3-D on the basis of their physical constraints. The result occurs on the basis of performance and analytic substance of every network individuallyfor the zero. In 3D-3D NoC system there is no redundancy of time. But 2D-3D arrangement can be opted for a larger network where power and time redundancy are the major barriers. By developing the 3D NoC structure the number of nodes is reduced while the data is transmitted from one node to another. The result shows that performance is improved by forty and thirty sex percent and the power consumption is decrease by sixty-two and fifty-eight percent respectively in 3-D NoC structure while the number of nodes are take one twenty-eight and two fifty-six respectively.

David. et. al in 2008 give his own views at the increasing complexity of multi core system, new paradigm introduced diverse Multi Processor SoC containing the typical intellectual properties, which transferthe data within the network at a very high speed. As the scalability of the hierarchy of buses is not

so good to embed the thousands of multi core processor. NoCs have been introduced to overcome the problem of complexity and scalability in shared bus architecture. The development of NoCs for multi-processor system on chip is very typical process that includes the different topological architecture to reduce complexity in terms of time and space. The author describes the benefit of NoCs using the synthesis flow of NoC and the analysis report on different implementation of the nanometer scale. Author presents the benefits of NoC in the field of area, consumption of the power and accessibility. Furthermore, there are also several fields are remaining to make the system more feasible design for Nano scale devices.

Mike Santarini in 2009 addressed two types of wired networks one is for computing and the second fortelecommunication. There are separate set of unique protocols for wired networks, there are different bandwidth requirement routing equipment and rate of bandwidth growth. There isa massive increase in the bandwidth requirement of telecom industry. A convergence of sorts took place, during the retooling of last wired networks which is marked by Goron brebner from Xilinx. Telecom and Ethernet both have increased their bandwidthrates. A line card is a combination of network processor unit, CPU, and the higher speed of a file programmable gate array. FPGA facilitates the communication between CPU and NPUs and NPUs are coordinated by processor to read data and route data. In future wired networks will be transferring internet data along with integration of all those IC packages.

Radu Marculescu et al. in 2009 focus on NoC architecture and its applications. Then they focused on 5 points of NoC relating to their research area which are NoC application classification, its transmission structure, transmission paradigm, their investigation, and theirsolutions for evaluation of their performance. Standard N-o-C design and its mapping to the NoC are described in this paper. They address the problems based on system, their micro architecture, and circuits.The internal structure of a node with on-chip router, processing

element and buffers are also described in this paper. In the paper it is also focused about the system level issues and infrastructure relating to communication. Major issue deals with the simulation-based methods which expresses that there is a trade-off between the simulation time and level of implementation. NoC combination movement containing the application prerequisite, NoC architecture, NoC confirmation and testing is described also.

Umit Y. Ogras. et al. in 2010 represents a mathematical model for on-chip routers which is based on the new model evolution of NoC performance and their analysis. This new approach not only gives the accurate result of the performance of the network on chip but also it provides the different NoC designing methods with in the optimization loop. They have shown the co-operated results based on the accuracy and practical consumption through their embraced result. Modeling and analysis technique are chosen for the multimedia traffic applied for the delayed studies. The described routing algorithm is a group of the buffer filled on the basis of first in first out phenomenon with 4 input packets through channels. Impending speed of router is explained through the concept of matrix which is diagonal based and the average gathering of the one packet is discussed through N input channels. The proposed algorithm also provides the feedback of the different characteristics of the network like as the average latency per router, the utilization of the buffer and the latency of the data flow. The proposed model is a work on the clock cycle which issynchronous. The router model should also consist the method to deal with the clock cycles with several domains.

Yang Quansheng. Et al. in 2010 proposed the T-mesh topology. A mesh NoC is the most popular topology which provides the complete solution to avoid the complexity on the system on chip. Still there is a back draw of transmission delay in the regular mesh NoC. The author proposed a regularTmesh topology model which is an improved version of the mesh

topology. The proposed topology consist the four more long link attached to the all terminal. Author suggested the routing algorithm based on the T mesh topology called Txy. By this algorithm the number of nodes while traverse the signal or data from one end to another end will reduce. The Tmesh is based on the algorithm Txy which make the system deadlock free through which data is transfer from one node to another node without any loop. The algorithm is not supporting to the concept of shortest path findings. That's why there exist many differences between the experimental results and theoretical results. Authors compared the results based on mesh and T-mesh from network diameter, throughput and average delay time. The experimental results show the reduction in nodes number and reduction in the average delay to reach the packet from one node to another node. Author applied the experiment for 8*8 nodes in the network and finds that there are reduction in the average delay is 2.92 percent and the reduction in nodes number approximately three percent less than as compared to the mesh NoC network.

Suleyman Tosun in 2011proposed a new paradigm on cluster based mapping from the point of view of integer linear programming. The method used for optimal solution is Integer Linear Programming (ILP) based mappings technique. Although, they suggested that method take more execution time. Authors have suggested ILP formulations method following the clustering technique. Many taste cases were tested following different custom graphs and multimedia benchmarks that were closer to achieve the optimal and closer solution within the range of tolerable period. At last after the experiment, the results indicates that the mapping on the cluster based is much better to map the different task in the distributed manner on chip network through which the accessibility become very easy and help to raise the speed of the transmission. The graph clustering methodology is same as the mesh clustering. The process of divide is repeated on the graph until the nodes of the sub graph cannot be

spitted further. To achieve maximum throughput, the graph clustering should be designed in the manner so that the flow of data among two clusters become minimum.

Ganghee. et al. in2011 explain about the 'coarse Grained Reconfigurable Architecture'. An application of multimedia and 3D graphics is used to analyze the result in this paper. The produced chips and applications drawn on CGRA show the performance and it has been found that the improvement in the performance is increase by one hundred and twenty times.

Jason cong. et al. in 2011 describe that the terms like energy and delay are needed to be more efficient while the data are transfer from one node to another node at the network on chip environment. The custom on chip network target on a given application. This is increased the efficiency as compared to the regular structure on chip. In this paper author proposed a tree topology phenomenon known as atree also written as ATNOC which helps to synthesize the network topology in which the pairs of nodes are connected through the links. From each module a router has maximum power consumption which is picked to minimize the consumption of the power and to decrease the latency. The reason to use the tree topology is that this topology is developed with shortest path, which help to reduce the path latency. A predict latency concept is prepared to predict path latency between the two intellectual properties. A method of temporal merging is used in this paper. In this paper both the models with temporal merging and without temporal merging are compared. The results off the experiments shows that the synthesize topology without using the bus and with using the bus reduce the power latency by forty-seven percent and fifty one percent respectively.

Aamir Zia. et al. in 2011 proposed an algorithm CNOC that is cloc network on chip. Authors developed the physical design and architecture for CNoC and compare it with other several topological structures on the behalf of several parameters

which used to judge the performance of a system. It is needed scalable and high performance communication infrastructure that provides the communication at low power. The paper suggested a closed Network on Chip (CNoC) architecture with the integration of the topological structure such as mesh, fat tree and flattened butterfly. The 3D NoC design was developed for 64 nodes and 512 nodes. It is analyzedthat the power consumption is increased when the size of 3D NoC was varied from 64 to 512. The system 3D- CNOC design takes 15 % less power consumption mesh, fat tree and flattened butterfly topology in comparison to other topology. The partitioning strategies, wire delay is also compared for these topologies. The 3D integration method is used to employ floor planning and partitioning and discusses their effects on wire delay. The 3D mesh structure utilizes minimum number of TSVs (9216) in comparison to the CNOC number of TSVs (10944). For the wire Length (mm) 10.5, 9.0, 7.5, 6.0, 4.5, 3.0, and 1.5, the power dissipation (mW), with respect to the same lengthis 1.74, 1.513, 1.306, 1.025, 0.8, 0.513, and 0.306 respectively, in case of plane wire. Thedelay (ps) is 287, 251, 208, 171, 128, 87.1, and 45.4 for the respective length of wire for plane wire. In the same way, power dissipation value and delay along interconnects is also analyzed. For the wire length (μm) 8, 16, 24, 32, 40, 48, and 56, the power dissipation (mW) is 0.014, 0.017, 0.018, 0.017, 0.021, 0.022, and 0.022. The delay (ps) corresponds to the same length is 0.017, 0.0212, 0.0281, 0.0453, 0.0505, 0.067, and 0.07.

ToshinoriTakabatake et. al 2011author discussed about the utilization of the several NoC topologies from the point of view of communication on the simulator. Authorpresent a new approach that is HCC known as the hierarchical completely connected. Authors compared this topology with the other network topologies and conclude on the behalf of the simulator that the performance of HCC topology is much better than the other NoC topological structure.

Ahmed Abousamra et. al (2011)asked about the concept of CMP (chip multi-processor) in which many task shared the

information from one node to another on the cache reside on the chip, so an effective transmission phenomenon is required among the cores at the chip as in the future hundreds or thousands of nodes will embedded on a single chip. NoC is the approach which provides the efficient communication among the nodes. In this paper the concept of two nodes based optical strategy used on the place of one node to make the result more efficient.

Wen-Chung Tsai. et al. in 2012 discuss the several common architecture and the techniques that deals with transmission performance, system scalability and power consumption in NoC environment. This article provides the information about architecture of the layered protocol. Author proposed the model of BiNoC that is also known as the bi directional NoC model. The number of channels between the two cores is not limited only up to two in the Bi NoC architecture. As the number of channels will introducethe performance will be increased. Every NoC router must have both hardware and software implementation as to support the functionality of these layers. The author also discuss about the Bidirectional channel that can improve the NoC performance remarkably with restructured NoC parameters. Eg: cost and power. Only two fixed unidirectional signal for conventional NoC and two bi directional channels signals for Bi NoC architecture are used while the comparison occur.

Yung-Chang Chang. et al. in 2012 authors have adopted to use 2D mesh and H-star topology to accompany a high performance switching architecture, and also proposed the work on Birkhoff-von Neumann (BvN) switching architecture. The architecture permits the resource bandwidth that depends on a particular traffic pattern. They tried to map a video object plane Authors developed system 'C' and cycle accurate model to probe further target NoC platforms into the dynamic. Author compared the experimental results and revealed that simple 2D-mesh network has traffic awareness algorithm for bandwidth allocation that overtakes H-star with

novelty and better connectivity. A real world application that is video object plane, a multimedia application also known as VOP is used.

Ciprian Radu. et al in 2013addressed on the problem of the mapping in the environment of the NoC. In this paper one operator that is mutual and two crossovers are proposed by the author. The problem of mapping is proposed in many objective ways. The objective of this paper is not only to minimize the consuming power but also make the NoC system thermally balanced. It has been proved by the simulator in this article that developed genetic operator enhance the utilization of the algorithm performance by using the domain knowledge edge on a real application.

Pradip Kumar Sahu .et al. in 2013 says that Application mapping is the new research issue in NoC. The cores of design for a particular application are mapped to the routers in NoC topology. It affects the power requirement and overall system performance. The paper focuses on the different mapping techniques employed in the last decade. The mapping technique is classified in dynamic and static. Static mapping approaches are further been classified as exact methods, transformative, constructive approaches and branch-and-bound. The performance comparison is also presented among static mapping techniques. Some test cases were generated that accepts 64 cores and 28 cores in the network. SUNMAP is a tool that is used applicable to map many cores of particular network and decides the best suitable to support the network architecture. It takes the available topology from its library targeting a particular application and synthesized the same topology. It explores the RTL design to attempt the design and minimizes design area, power dissipation and average communication delay and bandwidth. There is one of the most important compile is called Xpipes Compiler. It instantiates itself network components such as links, routers and interface specific to the topology. The greatest benefit of Xpipes is that it has highly parameterized components

based on specific structure. SMAP is used to map the network based architecture in MATLAB environment. XENoC is used to perform HW/SW design and complete the co-design to form an efficient distributed application MPSoC based NoC design. The MPS is used to targets fast and flexible design for space that performs evaluation of the mapped design used to decide greatest mapping for MPSoC based NoC design.

Amir-Mohammad Rahmani. et al. in 2013 describe that 3D NoC are used to provide lower power consumption in Multiprocessor interconnects, higher performance, improved packing density in comparison to 2D NoC. But there are some challenges which are not ignored such as power densities, peak temperatures, area footprints in vertical interconnects, higher peak temperature. The paper discusses the Bidirectional Bisynchronous Vertical Channels (BBVC) as area efficient architecture as power aware 3D NoC. Warm hole packet switching is used for data transfer and inter channel communication is also verified using VHDL based design. The simulation results revels that are footprint is reduced by 47 % through silicon via (TSV) and 18 % NoC power in their proposed architecture. For minimizing the power consumption, a concept that is dynamic frequency scaling used. The encoder for the 3 x 3 x 3 NoC was modeled and mapped. The clock frequency was decided of 200 MHz to perform interlayer communication for BBVC. The XYZ routing scheme was used. Several frequency at the particular interval of hundred are used for communication in interlayer. In comparison to the serialization methods, the suggested architecture has improved the requirements of power and average time for packet latency.

Haoyuan Ying et al. in 2013 describe that3D IC is becoming the most design issue and the 3D NoC are used to suggest the solutions based on yield, design complexity, and chip area. It can be used to minimize the number of TSVs, but it is a big challenge. The paper proposed routing algorithms which are suitable for 3D NoC environment to avoid the deadlock.

Authors proposed an algorithm for the routing based on system 'C' and simulated on GSNoC Simulator. They are also implemented using several routing algorithms using VHDL and power consumption is determined with the help of SYNOPSIS tool. The global frequency was set as 1GHz and the size of NoC to be developed of 8 x 8 in XY plane 8*8 in YZ plane and 8*8 in ZX plane and 4 x 4 in XY plane, 4*4 in YZ plane and 4*4 ZX plane respectively. All routing are deadlock free and follow adaptive routing. The proposed routing algorithms have achieved better performance in the comparison to the algorithm XYZ. The authors have proposed the methods of core placement and task mapping to get the better performance.

Eman Kamel Gawish. et al. in 2014 focused on the mesh NOC design and implementation of routing algorithm for variability tolerant. Many algorithms are proposed that provides lower probability of failure links in mesh network for variability tolerant perspectives. Different conventional algorithms like as XY, Negative first are discussedin the papers. The work is carried out in a tolerant and cycle accurate simulator NOCT weak. How the tolerant provides process variations to measure the performance of the NoCs. The result is shows that there are reduction in failure ratio of NoC is fifty six percent, while only three percent NOC failure rate is found while using the XY routing for variability tolerant. The results are obtained for a case of 8 x 8 mesh networks carrying random and uniform traffic for buffer size 16 at 45 nm and injection rate 0.1. The rate of NoC failure is increased with the increment in the number of nodes at the mesh NoC as well as there is the reduction in the size of buffer. The process variations are increased with the technology scale and the failure rate of NoC is also increased as well. Apart from it, different traffic size and patterns have different rates for NoC failure. The highest failure traffic rate has tornado, whereas the lowest NoC failure rate has traffic pattern neighbor. In the proposed tolerant variability routing uses static values

probability for link failures. The adaptive routing algorithms, such as even and odd, uses dynamic network conditions values probability for link failures.

Haytham Elmiligi. et al. in 2014 discussed that 3D NoC mesh architectures are the scalable architecture used to meet the requirements of low power consumption for multi core applications in larger scale. The research article discussed the 3D NoC applications methodology used to NoC mapping. The authors have suggested to use Genetic Algorithm (GA) is applied to understand the best mapping utilizes the minimum power consumption. The multicore architecture with 32 symmetric nodes is presented. All the nodes are running independently in homogeneous structure. The 32 nodes can exchange the data with the help of common memory unit. The core of the all the nodes is symmetric. A traditional algorithm known as Dijkstra's is used to determine the minimum path between the nodes. The suggested algorithm supports the minim power for the developed 3D mesh NoC. The proposed solution is beneficial for the design engineers to minimize the consumption of power while data transmitted in packet form with in the physical link.

Feng Weng et al. in 2015 describedthat NoC(Network on Chip) is an efficient but it experiences increasing leakage power. In order to remove the increasing power leakage, low power technique called power gating is being used but disconnection problem is one of the reasons which effect on network performance. Author proposed a way to avoid the disconnection. The asymmetrical bit splits the router into 2 different slices. Author introduced a concept that the slice may be divided into two Parts first part consume the maximum power while second part consume very less power. The slices which consume the wide range of power will cut off to avoid the leakage and slice which consumes very less power will be always active to avoid the power disconnection. By applying this phenomenon the power consumption can be avoid approximately twenty percent and as the result there are forty

four percent less power leakage. As technology scale drop down to deep submicron nanometer domain, the on chip communication is inclining on top. The on-chip consumes lots of power in multi-many-core system so it is important to use lower power technique. The low power gating phenomenon works at the level of router.

Ke Pang. et al in 2015 explore the different shapes of the NoC topology for different algorithm of task mapping. The concept of the task mapping is much effective from the point of view of reducing the consumption of the power and improving the performance of the timing. The flows of the mapping task play the important role to calculate the timing performance and energy usage on the platform of the NoC. This concept may be used for any algorithm regarding the mapping of task for any shape of the mesh topology. In this paper a 3 * 3 NoC shape is used for random benchmark mapping strategy.

Junxiu Liu. et al in 2015 proposed the ways to make optimal path selection called the EDAR algorithms. EDAR algorithms define different weight values. This paper also describe about a path routing algorithm for efficient data transfer using Efficient Dynamic Adaptive Routing (EDAsR) Algorithm. The strategy used in the paper is based on real time NoC traffic and weighted path selection approach using monitoring modules. The main objective is to maintain faulty and congestion conditions with the decisions based on effective routing. The status can be in ideal mode, busy mode, faulty mode or busty. The lowest weighted port is ranked as nearly optimized route to forward the packets. The method is applicable to by-pass the route for congested ports and diverts or tolerates the faulty ports. In the paper several traffic patterns are evaluated with the faulty or non-faulty nodes to access the throughput and latency to make fault free nodes. Under the different traffic load, congestion and injected faults, EDAR provides maximum throughput in comparison to other existing algorithms. In the addition of it, hardware area the overhead of EDAR is demonstrated in their research

to optimize the cost and design a scalable design of NoC for large scale. Multiplexers are used selected the different weights to provide the low area overhead. Adaptive routing structure is implemented using sum of different weights with preferred port, faulty, congested and busy. The output of EDAR is selected in east, west, north, and south direction to establish the connection between input traffic and output node.

Ran Manevich. et al in 2015 describe that as the number of hops will increase with growing the modular number the performance scalability of NoC topological structure will become the limited. It is happened because of the increasing in the number of hope which includes the long path as well as increase the number of routers in the path. The latency of the network is increased with increasing the number of hopes as the number of router is also increased. The hierarchical structure of the topologies may be one of the solutions to minimize the number of hopes as well as routers in the path. Author introduced a concept of active supervision of ordered NoC topologies.

Adesh. et al. in 2015 developed the NoC for ring topological structure. They followed the architecture based on rotator on chip architecture and token ring concept. The design was developed for 65536 nodes and following the concept of FIFO logic. The FIFO logic was used to provide the priority of service in the inter-process communication. The nodes were assigned the different nodes address each node can be serviced with the help of node address. To address 65536 nodes there is the requirement of 16 bit address used as source and destination address. Virtex-5 FPGA was targeted to synthesis the design and validates the results for inter process communication. The design supported the maximum frequency was 535.733MHz frequency.

Tahir Maqsood. et al. in 2015 presents quantitative assessment for mapping algorithms on NoC structure. It can be widely

vary with mesh sizes, task loads and communication system. Author concludes that 'communication aware packing based nearest neighbor' known as CPNN algorithm consumes less power. Although CPNN algorithm have higher communication overhead. Authors proposed an enhance model of CPNN technique that reduce the communication overhead. The discussed phenomenon was successfully developed at lower cost with the comparison to CPNN that is an effective solution of high scale mesh NoCs. Further the concept of patients was introduced with the NoC to carry the modeling and formal verification of designed NoC. It is concluded that it has the low cost, end to end latency, and hop count. The Communication-Aware Migration (CAM) algorithm has lesser power consumption than CPNN. Moreover, the suggested method has achieved 6% energy savings in case of smaller size mesh NoCs.

Majid Rezazadeh. et al. in 2015 describe that indirect topology can be designed and integrated in chip to support many conventional networks in multistage environment. The networks are applicable to minimize the hop count and can be integrated very easily integrated in a topological structure. In the paper authors have contributed to develop Multistage Interconnection Network (MIN) architecture under carbon nanotube technology (CNT) under synthesis traffic approach and track division. It is one of the architecture for future digital traffic technology. CNT is the promising technology for the future generation of the traffic networks, because it is capable to handle high densities of currents for a longer period without degradation in the performance, designed in next generation network chip and fabricated. Can all networks be feasible to provide a latest model as much they are efficient to provide maximum throughput? Authors have used the concept of data mining in the way to develop to develop a unified performance parameter. MIN structure provides the minimum delay, maximum bandwidth for DSP components and IP with memory units. The increasing bandwidth of the

pins can be utilized with the help of high radix routers. In a large scale network, as the numbers of components are increasing, the interconnection network provides the better performance and low cost to design the system. Clos, flattened Clos network, Benes networks, flattened Benes network, Omega network, flattened Omega network, baseline network, flattened Baseline networks are discussed in the paper. The simulation results of the paper show that CNT technology provides 30 % reduction in delay and 8 % deduction in power consumption. The throughput and message latency is increased significantly in comparison to conventional MINs.

Feng Wang. et al. in 2015 describe that in the many core technology, the main parts of the system are network on chips. It provides efficient and scalable architectures, which connects many chip resources. There is a crisis in the leakage power technology, which is further increased to scale down day by day. Power gating technology is used to mitigate the issues of leakage power. The problem of disconnection used in conventional NoC can affect the performance of network. In the research article authors tried to overcome the problem of disconnection using partial power gating. It avoids the performance loss of disconnections. Authors used the bit slice mechanism to distribute the routers into two slices. The data path architecture of the router is sliced into two parts and wider part is switched off using slices gating technique to save the power. All the narrow slices are kept active to avoid the problem of disconnection. Authors synthesized such traffic model to gain considerable amount of power at low load and performs better in comparison to the available router gated mechanism. The developed design was able to save 25.5 % power in comparison to the baseline design. It reduces the latency time by 45.00 % in comparison to the conventional power gated design. Authors claimed that power gating in bit sliced NoC technique provides better performance and power efficiency. The problem of leakage power can be mitigated with the help of power gating mechanism. Authors

have utilized the concept of FSM in modeling the traffic and synthesis their design. Bit slice technique was used to split the design into two parts asymmetrically and further partial power distribution approach was used. To construct a full subnet al narrow slice were used and gating mechanism used to save possible leakage power in wide slice. The slicing mechanism of narrowed on chip network and subnet in full connected form cannot perform the transmission of to normal packets.

Kamel Messaoudi. et al. in (2015) presented the codec H.264/AVC used for high quality video hardware chip. The hardware chip implementation is planned several codec processing elements (PE). The idea to implement codec is to provide SoC based solution so that system can work for multiprocessor system environment to integrate the different IPs. They proposed the 3 x 3 mesh architecture and then integrate the architecture with H.264/AVC in a particular network environment. The hardware architecture of H.264/AVC is implemented with the help of VHDL at RTL level. The results are simulated with the help of modelsim 6.1 software and the synthesis is carried with the help of Xilinx ISE12.2. The processing time of each block of pixel is calculated using simulated results. The overall system is designed using EDK tool on XUPV5 Xilinx support board. Same technique can be applied for inter decoding and inter prediction with a global system. The intra module was subdivided into two modules intra four by four and intra sixteen by sixteen prediction modules. They have used the inter prediction to provide connection in 16 x 16 module. The different modules for the synthesis H.264/AVC IP are 3 x 3 mesh NoC, intra 4 x4 prediction, intra 16 x 16 prediction, DCT & Quantization, inverse Quantization, inverse DCT, deblocking filter, Communication system (NoC + NIC) and IP resource for 3 x 3 NoC. The number of slice registers are 127/69120, 1477/69120, 2650/69120, 1821/69120, 1865/69120, 6702/69120, 2540/69120, and 14443/69120 with respect to each discussed module. The maximum frequency

of the utilization is 172.828 MHz, 278.431 MHz, 282.028 MHz, 594.107 MHz, 394.058 MHz, 188.638 MHz, and 165.781 MHz respectively to each module. The number of slice LUTs are 2154/69120, 1703/69120, 2180/69120, 1603/69120, 1712/69120, 8890/69120, 3226/69120, and 17242/69120 with respect to each module. Fully used bit slices are 5.89 %, 38.02 %, 49.33 %, 59.49 %, 38.70 %, 29.20 %, 0 % and 37.10 % respective to each module. BRAM/ ROM utilization is 0/148, 4/148, 0/148, 1/148, 1/148, 14/148, 6/29 and 29/148 with respect to each module. In the similar manner the number of DSP48E are 0/64, 0/64, 0/64, 16/64, 16/64, 0/64, 0/32 and 32/64 corresponding to modules respectively.

Prasad. et al. in (2015)proposed the Network on Chip (NoC) base d Fast Fourier Transform (FFT). The FFT is following the constable Geometry FFT transform (CG-FFT), parallel data, can process up to 8192 point reconfigurable structures. The large numbers of points are accumulated with the help of twiddle factor of the FFT and CORDIC algorithms. High throughput of the design is achieved using pipelined rotators of CORDIC. The signal flow (SFG) is used to under the different modules of FFT and help in the routing and network design. The latency of the FFT computations is reduced using SFG and optimizes the design of routers and network interfaces. The design was mapped to the mesh NoC and provides latency by 5 in the comparison to existing NoC architecture. The hardware utilization of the processing elements and different components of the network are synthesized on Kinetx-7 FPGA. The maximum frequency of the design of a PE in the suggested architecture was 184.010 MHz. The frequency meets the standards of timing parameters for DAB, 802.11a, DVB-T/H, and UWB. One PE with 8bits data width can occupy 2.595 mm^2area and consumes total power of 82.540 mW. The operating voltage is 1V to achieve these results. In the same way 4 port routers correspond to 16 bits data width was synthesized. The area occupied was 0.097 mm^2 and power was 15.717mW at 500 MHz frequency. The proposed

architecture has been designed with the help of VHDL and variable data rate is used to apply the same concept in several other applications.

Tassadaq Hussain in 2015 describe that the memory controller and the scheduling of the memory access are very much important in a multi core system. The system follows multiple memory units and task that enhances the delay, which affects the overall performance of the system. An efficient high speed scheduler and memory system is needed that is helping data access and its pattern to main processing core. In the research work authors have proposed Heterogeneous Multi-Core Memory Controller (HMMC) which is used to manage memory and scheduler. It can handle computational task and data movement. HMMC is coupled with the heterogeneous system that is used to provide the both application specific accelerators and general purpose cores. The designed and developed HMMC is tested and synthesized on evaluation board of Xilinx XC7VX485T FPGA VC707. HMMC can support regular and irregular access of memory. The experimental evaluation of the board supports the hardware utilization in which Xilinx Micro Blaze multi-accelerator and Xilkernel(RTOS) supports Multi-core System hardware resources. In the comparison to the baseline system, it is found the hardware utilization in HMMC is less by 43 %, dynamic power is less by 35.8 %, and speed improvement is 6.8 % and it can run multiple applications in real time.

2.2 Research Gaps

From the literature survey of the different authors it has been identified that the work has some gaps identified as

- NoC modeling is done for crossbar structures for 4 x 4 mesh NoC, 5 x 5 NoC etc. The research work is lagging with the implementation of the same mesh architecture that can support the functionality of 256 x 256 NoC structured

model or at a larger scale.

- In the same way, the ring NoC is also implemented for the limited number of the nodes and not explored in much way.

- The chip implementation of 2D NoC is done in large scale. There is very limited contribution to 3D NoC Chip and the performance estimation in terms of hardware resources and timing analysis.

- Further the research work can be enhanced to implement the same architecture on higher scale FPGA and validate the results after verify the internode communication.

- The comparison of the NoC design and their performance parameters can be a boon for VLSI industry. The performance parameters of the NoC design include minimum and maximum time, maximum output frequency, and hardware parameters such as resource utilization in terms of memory, logic gates, logic cells and no. of slices etc. My research work will focus on the implementation of the 2D and 3D mesh, torus, ring and tree NoC for large cluster size (N= 2, 4, 8, 16, 32, 128 and 256)

- The authors have not implement the chip of 2D and 3D mesh, 3D torus, 3D ring and 3D tree Topological NoC to support the large scale network (256 x 256 x 256) and perform internode communication

- The comparative analysis is not done yet to estimate that which topology is best for the future computer networks, wireless sensor network and existing wireless topology.

- Nodes communication and priority assignment or arbiter design for the 3D NoC for large scale networks is addressed by very less number of authors. Some discussed but for low size of networks only.