# INTRODUCTION

The chapter explains the introduction to Network on chip (NoC), Problem statement of the research work, objectives, Need and motivation to carry the research work. The research objectives contain the all supporting parameters for simulation and synthesis approach. The motivation and Scope of the research is also discussed in the end of the chapter.

## 1.1 **Introduction of Network on chip (NoC)**

Integrated circuits design and their manufacturing is completely depends on the integration of different sub modules which are the pre design block of the intellectual property (IP) and cores at single chip. The property of reprocessing is always resided in any ICs design. Manufacturing and semiconductors companies are working on the new challenges in the field of network on chip design and their throughput. The reuse of already developed sub modules or functional blocks is a new idea to design the circuits having high performance in shorter time period having larger gate counts. The developed design based on the discussed formalities is called as System on Chip (SoC). Traditionally the approach of System on Board (SoB) was used in which each block of the function is created and manufactured individually after that they mounted in a discrete board while now a days SoC used which has a single chip, in which all the cores are synthesized together. Later on the entire functional blocks are synthesized and manufactured in different units, and can be mounted in a discrete board. SoB is based on the already developed blocks. Moreover, the parts of SoC that can be reused are called virtual modules which are only used as the functional logics instead of fabricated ICs. It expresses a main comparison among the core based systems and traditional design methods.

The SoC core in present time have the integration of processors, networks, memories, analog interfaces, cryptography circuits,

input output devices etc. In the market, there are many companies of manufacturing IP. The functionality of the IPs is increasing day by day. The technologies are added in the products although the product time to market and design time reduced. The core based designs are extensively used in embedded based and related applications. The examples of such systems are portable medical disease equipment, Cell phones, automotive controllers and robots are suited example for the applications. The design and development time of the products depends on the technological expertise of the design, verification, signal processing, and security by encryption and decryption, RF design and analog interfaces. It is very difficult to predict that the technology has only the single house challenges. The chip size reduction, minimize power consumption, higher throughput, minimum delay, less area, reduced memory, fast response are the general requirements of these application. Moreover, it is the requirement that the all functions modules should be integrated in the system such as ADC, DAC, memory, microprocessors, mixed signal blocks etc. The business model is following the optimized design cycle to meet the requirements of application engineer, follow the RF or core solutions and focus on the basic system aspects.

It has been noticed in the manufacturing industries that the design time to develop the complex systems has been reduced because of the introduction of core based design. In the SoC based system the designers are able to address the new problems. Now the industries are focusing on design matrices such as time to market, design productivity time and they are also able to meet these challenges. But some parameters such as reliability, power dissipation and yields etc are the key issues in the current systems based on the core based on design or SoC. The testing of the ICs is one the area in which 50 % cost of the overall IC design and manufacture IC cycle is invested. In the early time it was 50 % to meet the requirements of the SoC. Since that time, the research was done to provide the efficient SoC testing and optimized architecture which can provide the mature and best plan for the testing of the complex systems.

The complex SoC designs require the system integration with parallel and pipelined approach, modular design approach, scalable architectures and testing in each phase of the design and production cycle. Then it will possible to understand the adequacy of these complex systems, solutions that can provide the use of NoC in interconnected platform.

Fault tolerance and reliability are the important keys for the future and current requirements of the SoC. It is not possible to predict NoC without SoC. The reliability of the circuits is defined by the test used and identifying manufacturing defects. The reliability of the faults is ensured by fault tolerance that is appearing in the general operation of system. First thing is that the quality and reliability must be considered of the NoC itself. The research in NoC is in the field of verifying the correct implementation, operation and manufacturing aspects of NoC. The NoC Characteristic are precluded the straightforward based on the fault tolerance and interconnections test. The first important characteristics of the NoC are that it has more wires to connect or density of wire is large in comparison to the bus architecture. Another characteristics is relating to manufacturing of the NoC. Some defects can be identified based on high density structure and the nanometer processes and high density structures especially sensitive crosstalk, some defects and large range which are common in most of the communication technologies and their architecture chip. The communication in such architecture is not possible only by wires but the multiple blocks of wires are required. In the addition of this, these wires are not accessible easily and directly as happening in bus based architectures. The nodes in the NoC are accessed using routers with the help of Network interface (NI), core or channels. So, the testing of all these parts relay on the need of each other and it makes the process much complex.

## 1.2 **Problem Statement**

The problem statement of the research work is given as

**"Network on Chip (NoC) Implementation for 3D Network Topological Structure in HDL Environment"**

## 1.3 **Objectives**

The objectives of research are defined to complete in two phases, First phase is the system design and second phase is simulation and verification. The objectives of the research work are given as

- Design and chip implementation of 2D fat tree, mesh, torus, and ring topological NoC
- Design and chip implementation of 3D mesh, torus, ring and fat tree topological NoC
- Functional simulation and analysis of 2D and 3D fat tree, mesh, torus, and ring topological NoC
- Verification and validation of optimal design on FPGA.

## 1.4 Need and Motivation

The current SoC system design and development depends on the most of the factors such as time to market and design time. The current semiconductor and computer networking companies are looking towards the fast and reliable design and solution in the field of computer nodes communication and technology using the single chip. The chip performance is estimated by many parameters such as delay, frequency of operation, power consumption, chip areas and real time system. Dozens of the functionality of the system depend on the power requirements and frequency. The power is completely related to the hardware and memory resources utilized by the system itself. Network on chip is the network version of the chip based SoC working in multiprocessor environment. When the multiple nodes want to communicate in a real time environment, there is the required of scalable

and feasible architecture which can be reprogrammed and used instead of the failure of anyone of the node. When multiple nodes are communicating in the real time, they are arranged in the specific topology. The topology is categorized as direct or indirect. The examples of direct topology are ring, tours and mesh. Mesh is the highly used topology in the NoC Communication. The 2D mesh torus topology follows the XY routing and 3D mesh and torus topology follows XYZ routing. The current manufacturing companies are looking for the dependability and reliable solution for NoC. Another important feature is that weather the network size is expandable in terms of nodes. The NoC chip time to market time depends on the design time of the NoC. If the designed time is taken a lot to launch the particular NoC in the market, then there is no use of the research and meet market time.

There are many wireless technologies such as Zigbee, Bluetooth, Wifi etc. All the wireless technologies are controlled by the wireless chip and used for node to node communication. All the wireless technology supports the specific topology. For an example the Zigbee wireless technology supports the mesh, star and cluster tree topology. When these wireless modules are placed in wireless sensor networks such as in disaster area, specific field, agriculture fields. It is required to communicate with multiple nodes. If this communication is done with a controllable chip integrated with high speed FPGA. It is one of the best solutions of the existing system working on microcontrollers based on monitoring. As discussed the wireless modules are working in specific topology. If we are able to develop the chip to control such environment, it will be a great research. Another aspect is that the existing research on chip is done on 2D topology for small scale of the network, not for a large scale networks in which we can control multiple nodes. To energies so many number of the nodes, power is required. We can also analyzed the system based on power and hardware used so we can estimate that which topology is best suited for specific applications.

Traditional systems are based on the bus communication

which has limited number of wires to the nodes and dedicated link in case of the failure the communication among nodes is not possible. If we will choose the NoC based solutions nodes have alternate path to communicate because the NoC can configured in multistage and multilayer environment. NoC are working in chip core as IP cores which have many wires

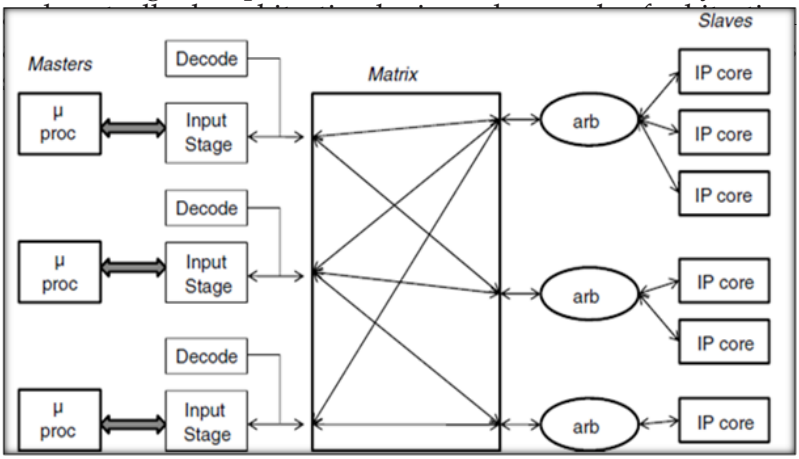


**Figure 1: Matrix architecture and multiprocessor environment**

Traditional systems are based on the bus based communication which has limited number of wires to the nodes and dedicated link in case of the failure the communication among nodes is not possible. If we will choose the NoC based solutions nodes have alternate path to communicate because the NoC can configured in multistage and multilayer environment. NoC are working in chip core as IP cores which have many wires and controller by arbitration logic, and example of arbitration and optimized matrix in multiprocessor environment as shown in [Figure 1].

The data flow control is relating to the data traffic or intensity inside the routers and in the channels. Routing is a technique or method that defines the optimized path between a data or message to take place from the transmitter to the

target end or receiver. The arbitration mechanism assigns the scheduling or priority of tasks or set the rules when multiple devices want to communicate with master device at the same time or multiple messages are requested by the same node. Switching is the techniques that defines how an incoming traffic is accepted by a router and send to the output port of router. In the last, buffering is the approach used to store messages or data and process while the output channels are busy. Hence large scale NoC design depends on the routing, flow control, switching and buffering.

### 1.4 Structure of thesis

The structure of thesis can be understood with the help of following discussions.

- **Chapter -1** is based on the introduction to NoC, Problem statement, objectives, need and motivational work and Scope of the research work.
- **Chapter -2** is based on the detailed literature survey done on the different research work based on the problem define in chapter -1 and what are the finding with the review of each paper, is continued in Chapter with identified research gaps.
- **Chapter-3** is based on the functionality of different NoC topologies. The chapter explains the basic concepts of network topology and different topological structures used in network communication.
- **Chapter 4** focuses on the designing of 2D and 3D mesh, ring, tors and fat tree topological configuration cluster size. The chapter also discusses the addressing and routing schemes for all NoC architectures
- **Chapter 5** describers the simulation and synthesis tools environment to development the design and research methodology. VHDL programming language environment is used to develop the chip.

- **Chapter 6** is based on the results and discussion part. It includes the comparisons between design and simulated parameters extracted from Xilinx software, a detailed discussion is carried out to compare the results of 2D and 3D mesh, torus, ring and fat tree to predict the optimal design.

- **Chapter 7** is based on the Conclusion based on the results and future scope of the research is also discussed in chapter 7 and the thesis is ended by with the help of the references and Appendix supporting to carrying out the research work.