About the Book

The solution for the multiprocessor system architecture is Application specific Network on Chip (NoC) architectures which are emerging as a leading technology. Network on chip (NoC) architecture is an approach to develop large and complex systems on a single chip. In this work, 2D and 3D mesh, torus, tree and ring topological structure has been implemented in Very High Speed Integrated Circuit Hardware Description Language (VHDL). The hardware utilization and related parameters such as slices, flip-flops, LUTs and Input and output blocks IOBs of 2D mesh, 2D torus. 2D ring and 2D fat tree topology is increasing with the increase in network configuration or the cluster size of the network (N= 2, 4, 8, 16, 32, 64, 128, 256). In the same way, all the parameters for time values are also simulated such as min time and max time before and after clk, min period, and frequency of operation. The timing values are estimating the performance of the design. The simulated and verified results analysis is done for each topology for cluster size (N= 2, 4, 8, 16, 32, 64, 128 and 256). It is concluded that the mesh NoC has the optimal design based solution in terms of hardware resources utilization, timing result, and memory. It is also analyzed that the space or area required for the designing of mesh topology is less.

About Me

Dr. Jain is Associate Professor at Teerthanker Mahaveer University, Moradabad, India. He has more than 15 years of teaching and research experience. In his 15+ years of experience, he has been able to bring out best from individuals and create a healthy work environment, With the changing work demand. He has been able to write about more than 20 research papers including the SCI Journal, Scopus Journal, UGC Care List, Web of Science, Thomus Reuters on topics ranging from Digital Image Processing to Network on Chip Implementation with a backdrop of improving the Chip performance and utility. He has also filed the 10+ patents on National and International level. His Research areas are Digital Image Processing, Maching Learing, Convolutional Neural Network and Chip Implementation.

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NETWORK ON CHIP (NOC) IMPLEMENTATION FOR 3-D NETWORK TOPOLOGICAL STRUCTURE IN HDL ENVIRONMENT

DR. ARPIT JAIN

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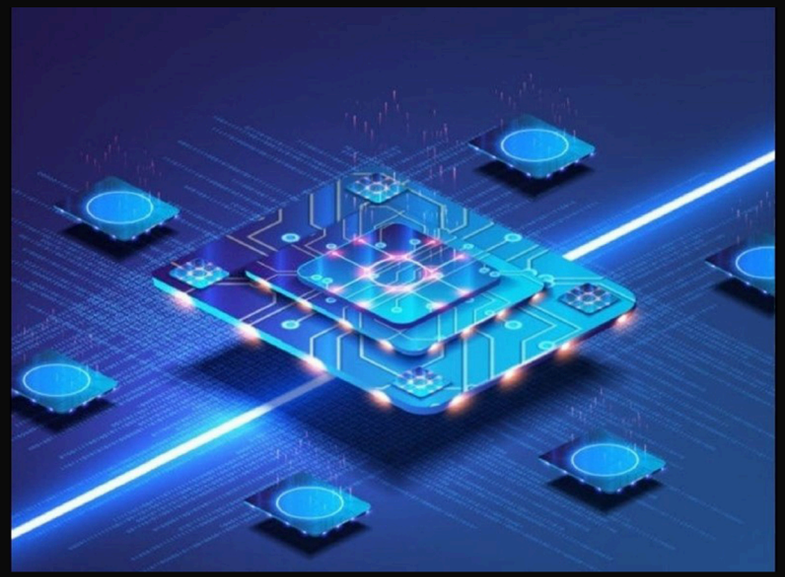

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