ABSTRACT

The solution for the multiprocessor system architecture is Application specific Network on Chip (NoC) architectures which are emerging as a leading technology. Modeling and simulation of multilevel network structure and synthesis for custom NoC can be beneficial in addressing several requirements such as bandwidth, inter process communication, multitasking application use, deadlock avoidance, router structures and port bandwidth. Network on chip (NoC) architecture is an approach to develop large and complex systems on a single chip. NoC is the network version of the MPSoC. A NoC can be structured and arranged by its topology with the completer organization of the routers and cores and the approaches used to understand the technique for routing, arbitration, buffering, flow control, and switching. The data flow control is related to the data traffic or intensity inside the routers and in the channels. Routing is a techniques or method that defines the optimized path between a data or message to take place from the transmitter to the target end or receiver. In this work, 2D and 3D mesh, torus, tree and ring topological structure has been implemented in Very High Speed Integrated Circuit Hardware Description Language (VHDL). The research work focuses on the modeling, simulation and synthesis of mesh and ring topological network. The cluster size of the network is considered as (2 x 2) , (4 x 4), (8 x 8), (16 x 16), (32 x 32), (64 x64), (128 x 128) and (256 x 256) for 2D NoC design and (2 x 2 x 2) , (4 x 4 x 4), (8 x 8 x 8), (16 x 16 x 16), (32 x 32 x 32), (64 x 64 x64), (128 x 128 x 128) and (256 x 256 x 256) for 3D NoC design. The work is carried out in Xilinx 14.2 Software and modules are functionally simulated in latest modelsim 10.0 student edition software. The chip design are tested well on Virtex 5 FPGA and validated in the same hardware by the experimental work. The router is used to forward the data packets in communication network. The data packets are transferred form one source router to another

destination router in the internetwork. The communication among the nodes in all topology is done based using 2D and 3D routers. 2D router accepts the data from 5 ports such as east_input_output, west_input_output, north_input_output, south_input_output, and local_input_output. 3D router accepts the data from 7 ports such as east_input_output, west_input_output, north_input_output, south_input_output, Up_input_output, down_input_output and local_input_output. The data communication in all the NoC structures are simulated and verified for 256 bits. The router design, FPGA implementation of 2D and 3D mesh is scalable in comparison to other topology. The regular design and structure feature of the mesh NoC is the greatest attraction of all designer because there may be another possible link in case of the failure of the specific link for internode communication. Nodes are placed on the equal distance and address by XYZ routing. The hardware utilization and related parameters such as slices, flip-flops, LUTs and Input and output blocks IOBs of 2D mesh, 2D torus. 2D ring and 2D fat tree topology is increasing with the increase in network configuration or the cluster size of the network (N= 2, 4, 8, 16, 32, 64, 128, 256). In the same way, all the parameters for time values are also simulated such as min time and max time before and after clk, min period, and frequency of operation. The timing values are estimating the performance of the design. The simulated and verified results analysis is done for each topology for cluster size (N= 2, 4, 8, 16, 32, 64, 128 and 256). It is concluded that the mesh NoC has the optimal design based solution in terms of hardware resources utilization, timing result, and memory. It is also analyzed that the space or area required for the designing of mesh topology is less. One more reason is also that the topology grows almost in the linear nature with the increment in the number of the nodes in XY and XYZ for 2D and 3D. The advantage of the mesh topology over the other is due to its structure linearity and physical design. The chip modeling and design of mesh and ring topological structure is a boon for the VLSI industry because it integrates the concept of multiprocessor in a single

chip. The Register Transfer Level implementation, extraction of hardware and memory parameters and comparative study will help the designer to understand the feasibility of interfacing the future system on chip (SoC) and network on chip (NoC) based solutions.